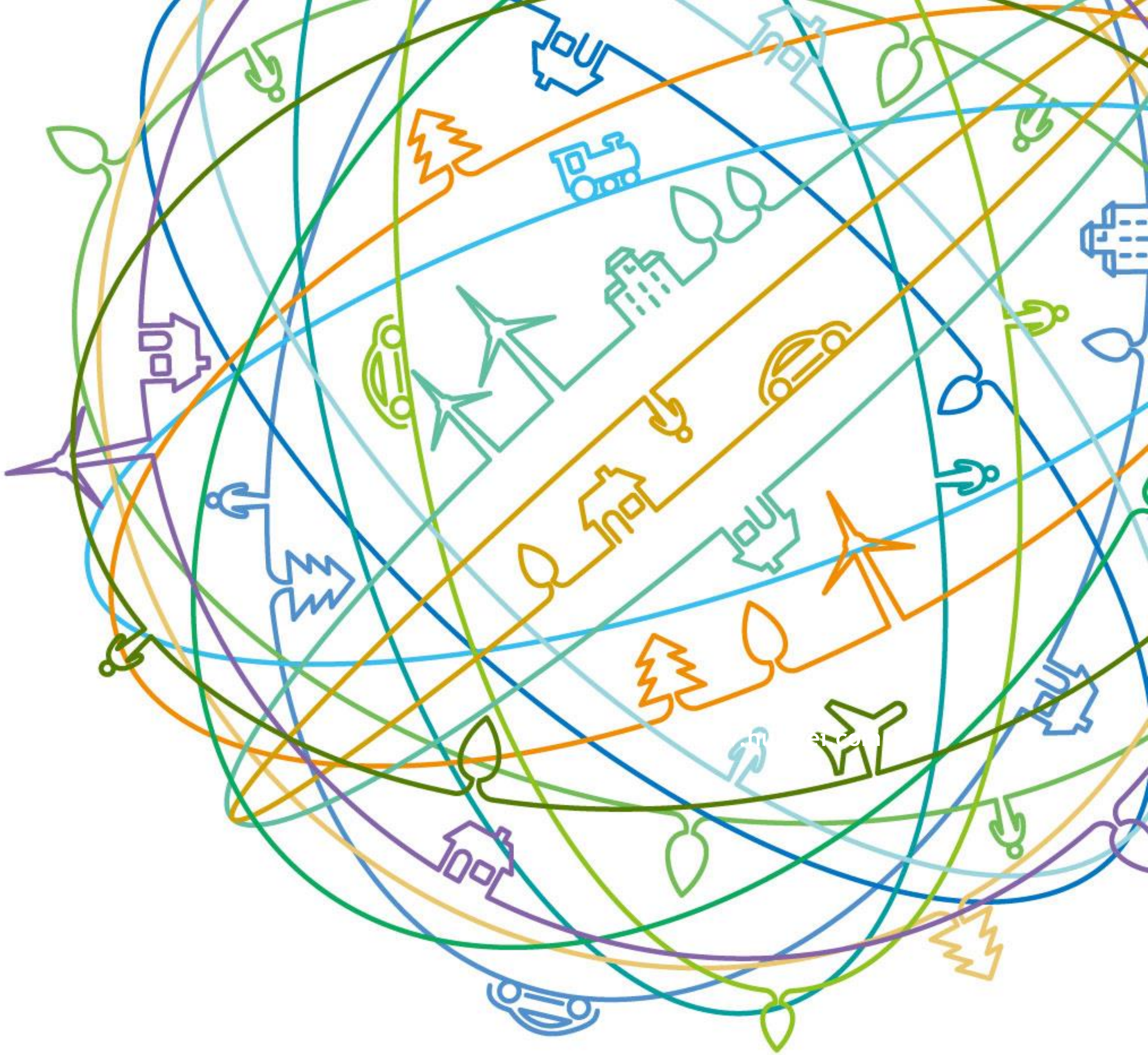
Debriefing the Open Innovation Platform for UnifiedBus



Wenjia Wei

Huawei, Network Technology Laboratory

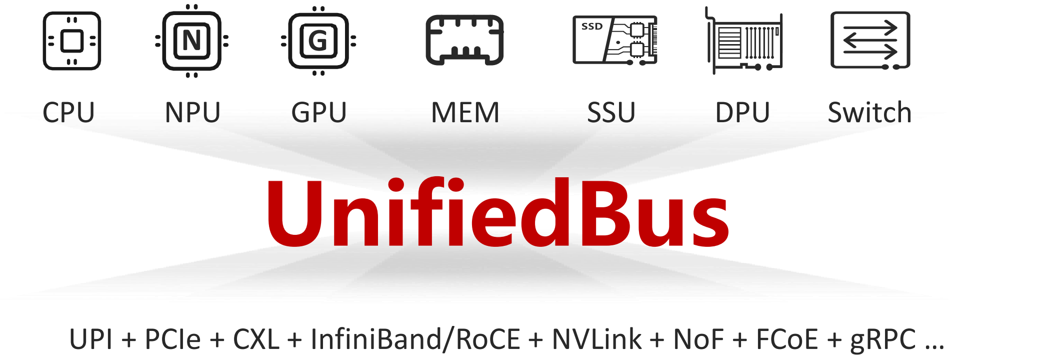
UnifiedBus: An Interconnect Protocol for SuperPoD

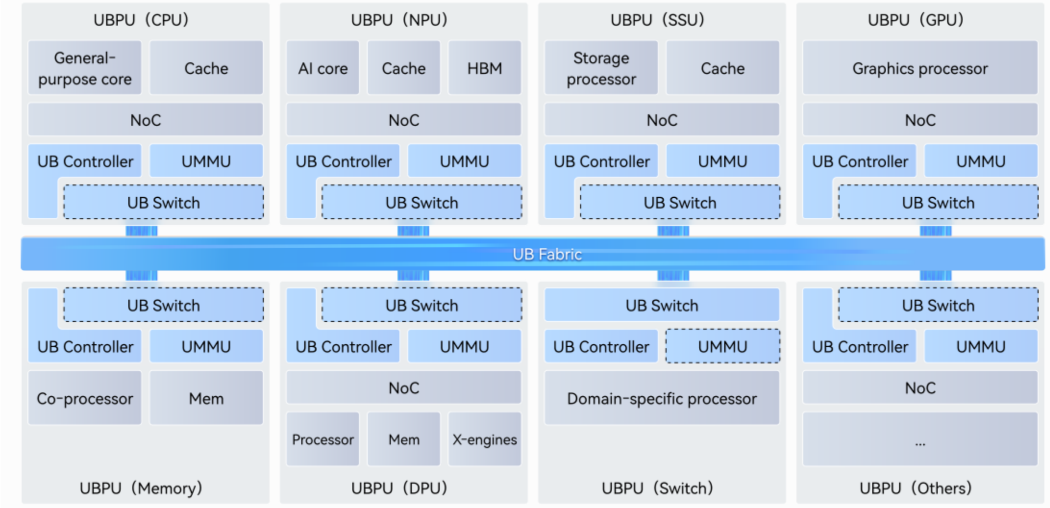
UnifiedBus (UB) is a SuperPod-oriented interconnection protocol that unifies IO, memory access, and inter-process-unit communication.

Key Capabilities:

- **Low Latency:** any port can connect and forward to any type of devices without protocol conversion overhead.
- **Higher bandwidth:** all high speed SERDES can be utilized for any purpose, maximizes resource efficiency
- **Simplified Schema:** Load/Store + RDMA + uRPC.
- **Compatibility:** UBoE can run natively over Ethernet Network

A unified interconnect to cover common bus & network scenarios.





UB Domain Diagram

We Build Innovation Platforms Together with the Academic Community

The First Systematic Open Innovation Platform Designed for SuperPod Networks

Driving innovation in architectures, protocols, algorithms, memory semantics, and programmable hardware.

UB Simulation Platform

UB Protocol Verification Platform

Scale-Up Prototype Platform

SuperPod Networking Innovation Platform

Scale-Out Prototype Platform

香港科技大學 THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

Jointly released with academic partners

Openness · Innovation · Collaboration · Success

UB Simulation Platform:
A UnifiedBus Specification Compliant Network Simulator

Supporting research into the following areas:

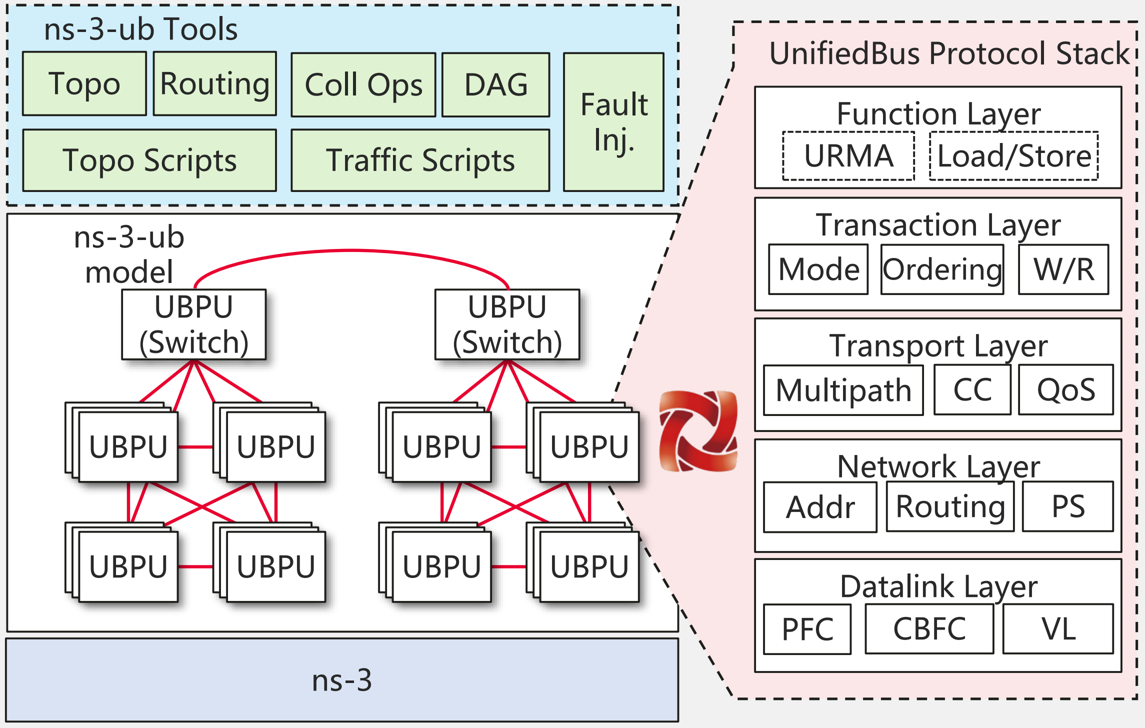
- High-reliability, low-cost, traffic-affinity topologies.
- Optimization for collective communication ops.
- Novel transaction ordering and reliability mechanisms.
- Transmission control mechanisms for Ld/St semantics in SuperPod.
- New adaptive routing, LB, CC, and QoS algorithms.

Integrated Tools:

- Flexible topology generation (e.g., CLOS, UB Mesh).
- Custom traffic injection (supports collective ops).
- Node/link fault injection.
- Simulation log analysis and data visualization..

Access:

- Base on ns-3.44. Repo: https://gitcode.com/open-usim/ns-3-ub



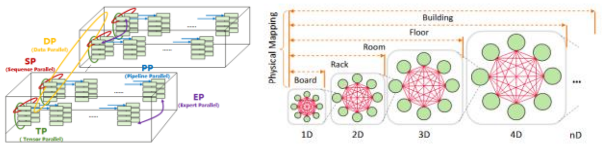
ns-3-ub Architecture Diagram

This project provides reference implementations for algorithms not defined in the specification (e.g., switch modeling, congestion marking, buffering, and arbitration). Features out of scope: hardware modeling, physical layer, control plane behaviors (e.g., initialization, exception handling), memory management, and security policies.

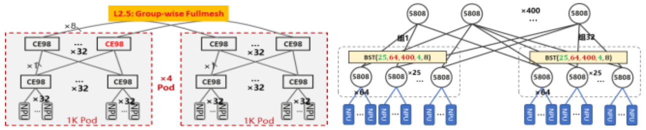
Supporting Research Areas:
Architecture Exploration, Protocol Innovation, and Algorithm Design

Innovative Topology Architectures

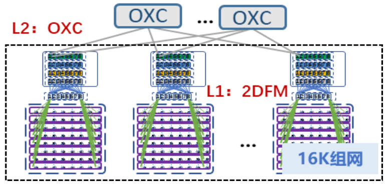
UB Mesh Performance Evaluation



Sparsely Connected Topologies



Electrical + Optical Topology



Innovations in Protocol Stacks and Algorithms

Memory-Semantic Innovation

Transport Layer

- In-Order Delivery of Pkt.
- Reliable Trans.
- Load Balance
- Congestion Control

New TA Layer

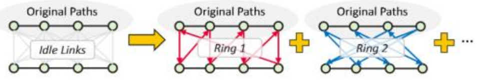
- In-Order Exec. of Inst.
- Transaction Reliability

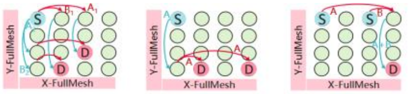
Compact TP Layer

- Load Balance
- Latency & Sending Rate Ctrl.

Innovative Collective Algorithms

Multi-Ring AllReduce

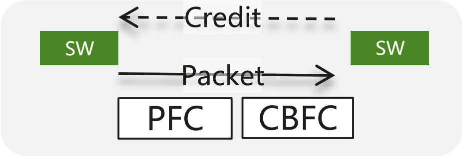




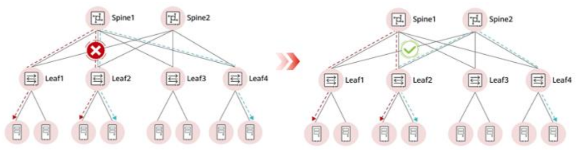
(a) Multi-Path All2All (b) Hierarchical Broadcast (c) Hierarchical Reduce

Multi-Path and Hierarchical All-to-All

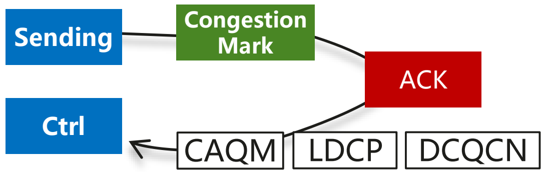
Traffic Control Innovation



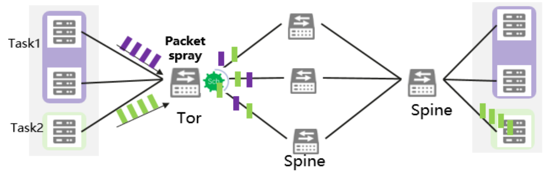
Network-Level Load Balancing



Congestion Control Algorithms



Packet Spraying & Adaptive Routing



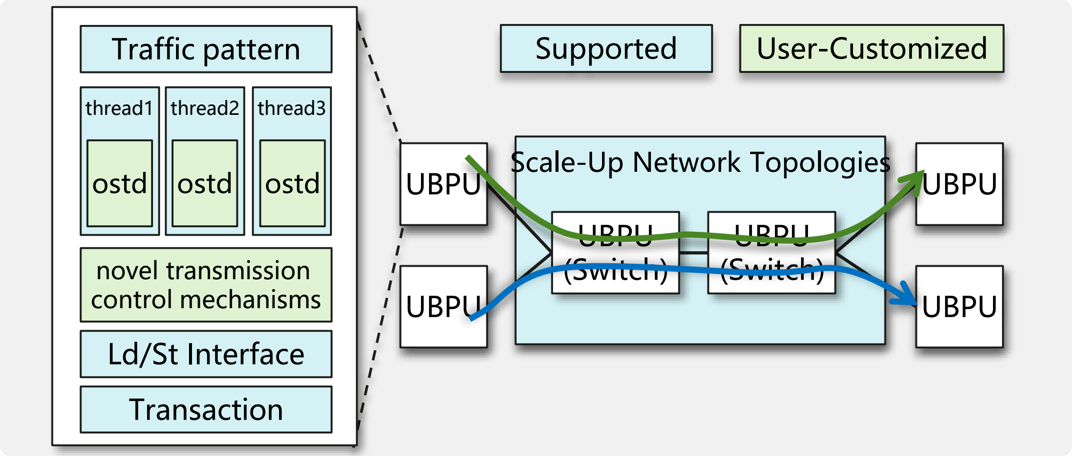
Simulation Framework Innovation

Case 1: Memory Semantic Innovation

- Utilize LD/ST interfaces to generate complex traffic patterns to evaluate the strengths and limitations of existing transmission, ordering, and reliability technologies.
- Enables users to design and validate innovative mechanisms tailored for AI traffic and specific topologies.

Novel Transmission Control Mechanisms

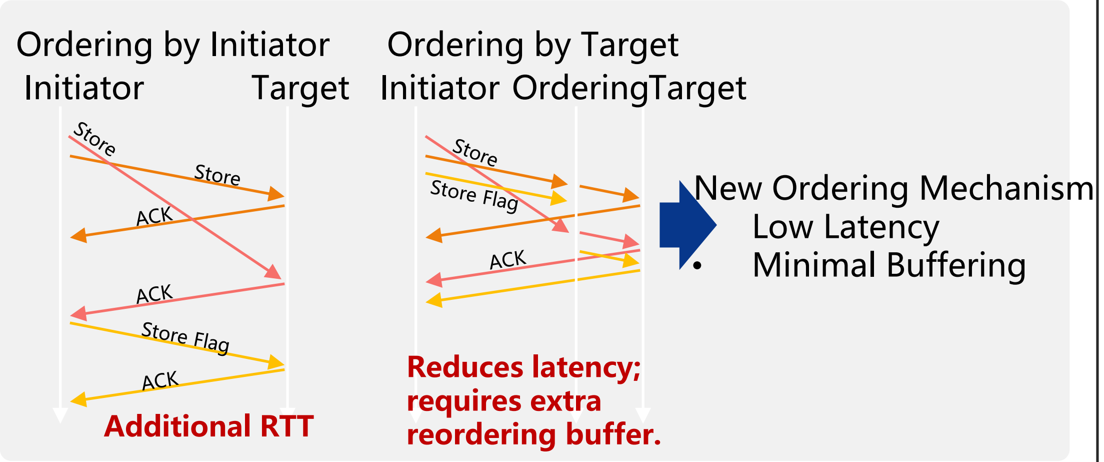
- In memory-semantic scenarios, transmission uses a lightweight protocol stack that bypasses the transport layer.
- For future larger-scale, complex scale-up networks, new lightweight transmission control mechanisms are needed to meet control requirements.



Design novel transmission control mechanisms for SuperPods and scale-up scenarios.

Network-Level Transaction and Reliability Innovation

- Straightforward ordering implementations suffer from additional RTT latency and buffering overhead in ROI/ROT transactions.
- Design novel ordering and reliability schemes to ensure lightweight, high-efficiency transmission.



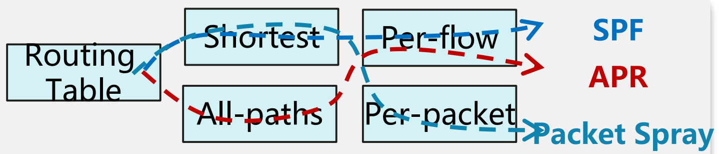
Develop novel reliability and ordering schemes to boost transmission performance for scale-up scenarios.

Case 2: Network Architecture & Algorithm Innovation

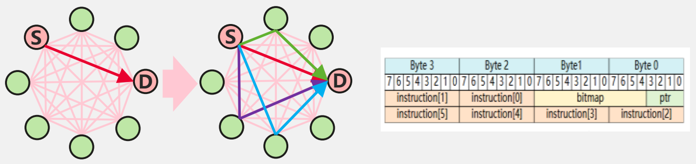
- Build any network topology to investigate novel architectures tailored for AI training and inference scenarios.
- Design innovative routing policies, collective communication algorithms, and flow control mechanisms based on new topologies.

Routing Mechanism

- Supports UB protocol-defined routing strategies.
- Design custom algorithms for innovative topologies.



Supported Routing Strategies

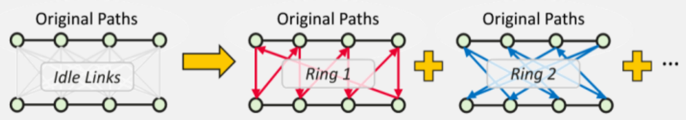


UB-Mesh Source Routing Strategy

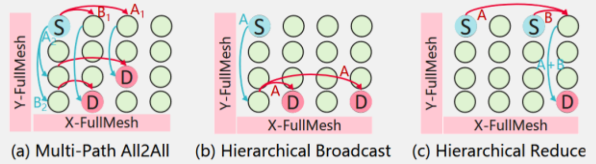
Supports extensive routing strategies and enables user-defined mechanisms tailored to specific topology.

Collective Algorithm Innovation

- Generates standard algorithms and injects traffic in arbitrary serial/parallel patterns.
- Allows users to design and simulate custom algorithms based on specific topology and traffic needs.



UB-Mesh Multi-Ring AllReduce

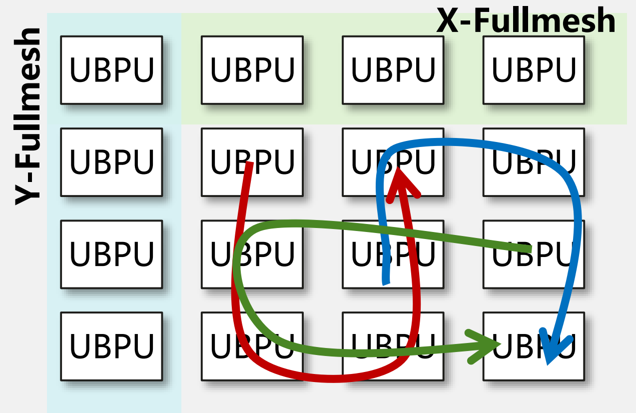


UB-Mesh Multi-Path and Hierarchical All-to-All

Validates innovative algorithms using tools to generate arbitrary traffic types.

Flow Control Algorithm Innovation

- Supports CBFC/PFC and Virtual Channels for verifying flow control and deadlock prevention.
- Enables deadlock reproduction and resolution algorithm design.



Reproduces deadlocks and analyzes root causes via logs; resolves issues using Virtual Channels.

UB protocol Verification Platform: The Verifier for UnifiedBus Protocol Designing

Supporting verification in the following areas:

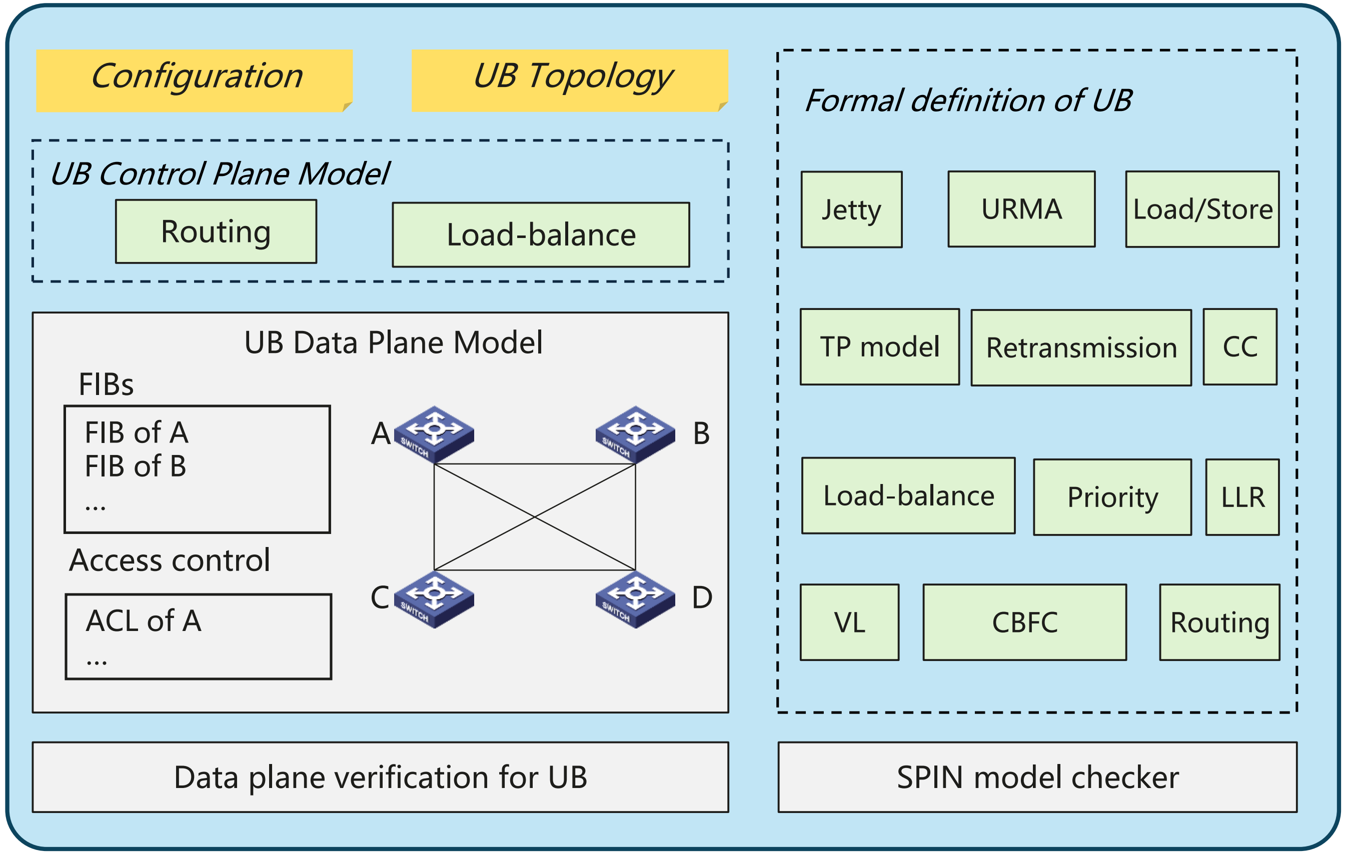
- Correctness of protocol designs.
- Correctness of configurations.
- Compatibility of new designs.
- Robustness of control plane algorithms.

Usage:

- By defining new protocol designs in this platform, the verifier can automatically verify their correctness.
- By inputting the deployment configurations to this platform, the verifier can determine the correctness of configurations and compatibility between protocols.

Access:

- Repo: https://gitcode.com/open-uvfy/ub-NetVerify



Supporting Research Areas: Protocol Design and Control Plane Algorithm Design

Support for Innovative Protocol Design

- The platform contains complete formal descriptions of the main features of the UB protocol, as shown below.
- New protocol designs can be verified on this platform by modifying the formal description.

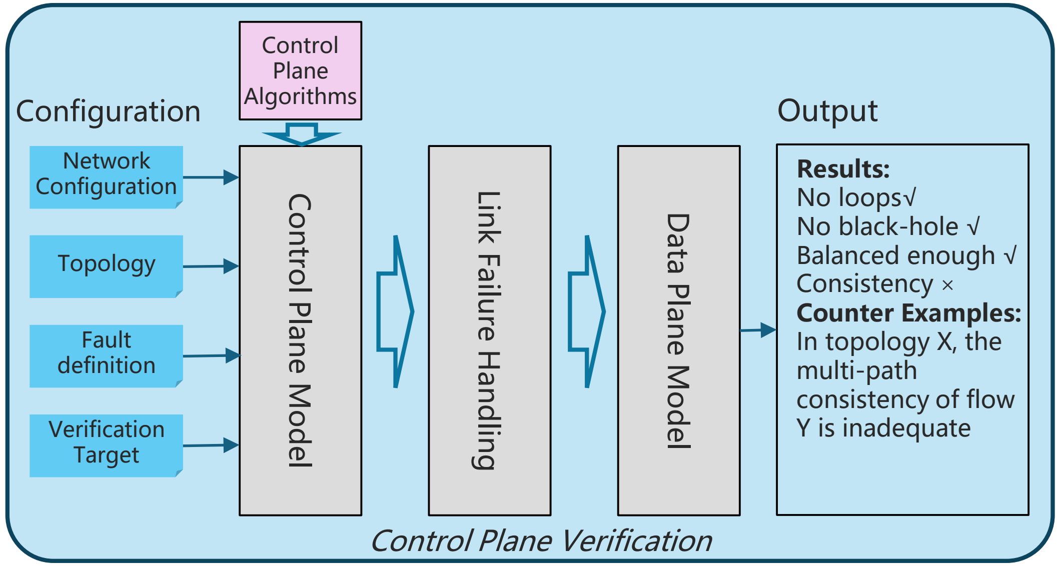
Protocol Layer	Protocol Function	Verification Features
Datalink Layer	VL&CBFC	Correctness and deadlock-free of credit subscribe and release.
	LLR	Correctness of state transition and error handling.
Network Layer	Routing	Correctness and compatibility of routing.
	Isolation	Effectiveness of the isolation strategy and correctness of isolation.
	Priority	Starvation detection and conflicts detection.
Transport Layer	TP model	Correctness of state transition and reliability function.
	TP	Correctness of transmission process.
	Retransmission	Detection of packet loss status and packet loss deadlock.
	CC	Congestion control process verification.
Transaction Layer	Jetty	Correctness of Jetty state transition. Jetty abnormal state detection.
	URMA	Correctness of URMA interaction process and state transition.
	Security	Correctness of the security state space.
	Load/Store	Correctness and deadlock-free of memory transactions.

Support for Control Plane Algorithm Design

- **Verification of load balancing and packet reordering in the control plane.**

The platform can verify the balance and multi-path consistency of innovative control plane algorithms under the following situations:

- Different topologies, such as UB-mesh, CLOS, etc.
- Link failures.
- Different traffic characteristics.



SuperPod Networking Innovation Platform: Support innovative UB topology construction and verification of topology designs.

Capability Features of the platform:

Infrastructure

Ascend / Kunpeng Servers, OCS, Electrical Switches

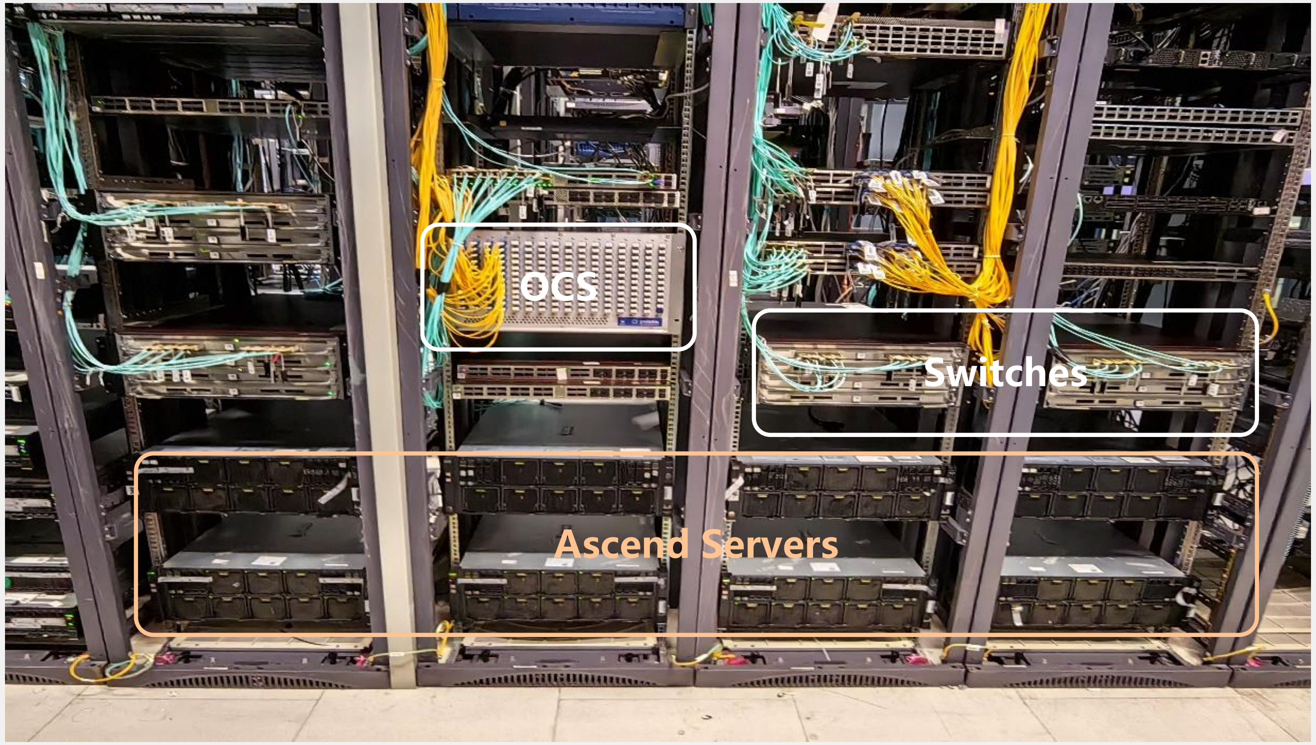
Feature 1: Innovative Topology Definition and Construction

- **Direct topologies (FullMesh, 2D-FM, Torus)**
- **Indirect connection topologies (Clos, BST, etc.)**
- **OCS-based variable direct topologies**
- ***Provides more accurate performance evaluation and realistic problem identification compared to simulators***

Feature 2: Verification of Topology Algorithms

- Routing algorithms (shortest path routing, full-path routing), LB algorithms (ECMP, NSLB, etc.), FC algorithms, and collective communication algorithm configurations under various topologies.
- ***Supports Python-based HCCL translation.***

Networking Innovation Platform: Supports customized interconnection of Ascend servers, switches, and OCS hardware, and integration, configuration, and verification of routing and communication algorithms.

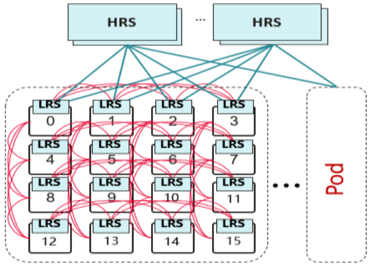


Access: Huawei will assist in configuring and setting up the network, with remote access provided via the Huang Danian platform and the laboratory.

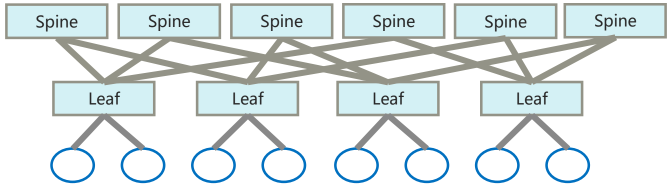
Innovations in UB SuperPod Topology Architecture, Routing, and Communication Algorithms

SuperPod topology innovation

Supporting UB-mesh topology (Example 1) and innovative switching topology (Example 2) prototype development.



Example 1:
UB-mesh Topology

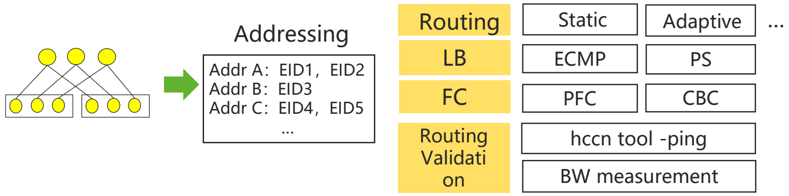


Example 2:
Balanced Sparse Tree Topology

Flexible and customized definition of Topology

Innovations in Routing and Collective Communication Algorithms

Supports efficient configuration of source routing and static routing;
Innovative routing algorithms (full-path routing).



Translating Python algorithm code to HCCL collective communication library supports efficient and agile innovation and development of communication algorithms.

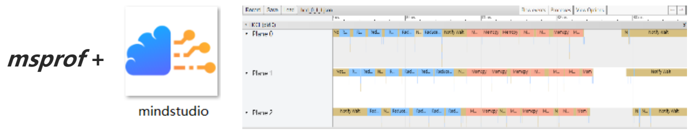
Python → HCCL Ascend

https://gitcode.com/HCCLang/HCCLang-ub-tools

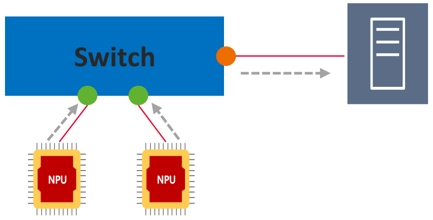
Agile Development of Innovative Algorithm

Network data monitoring, platform data visualization

HCCL Operator Behavior Data Collection and Visualization on Device-Side (Ascend NPU)



Network-side port mirroring, "flow-level/packet-level" traffic behavior observation strategy



Data transparency, facilitates academic and industry research.

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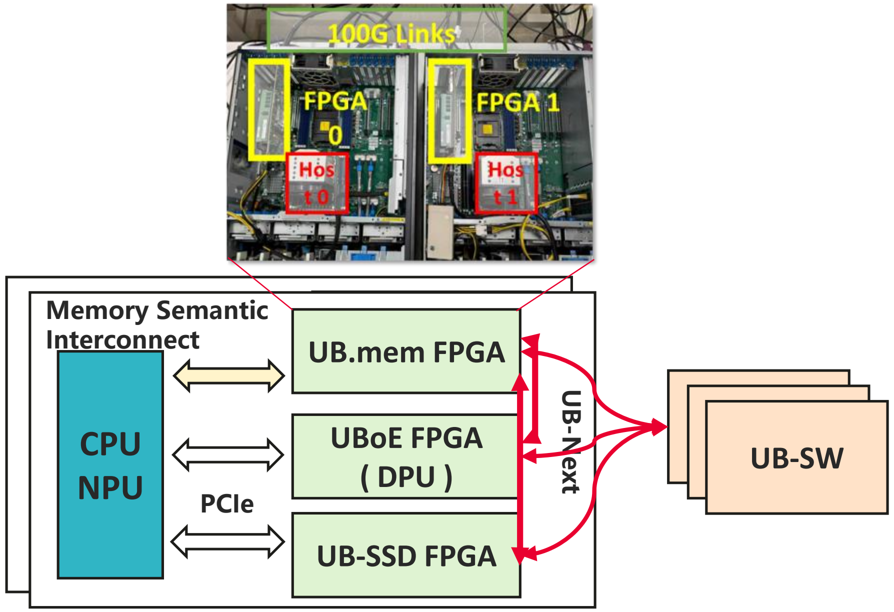
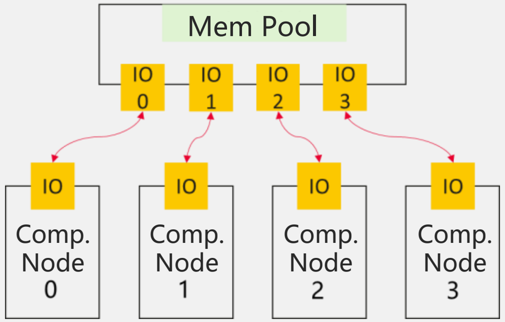
Scale-Up Prototype Platform: Open HW/SW Co-Design Capabilities to Support Innovation in UnifiedBus Interconnect Architecture

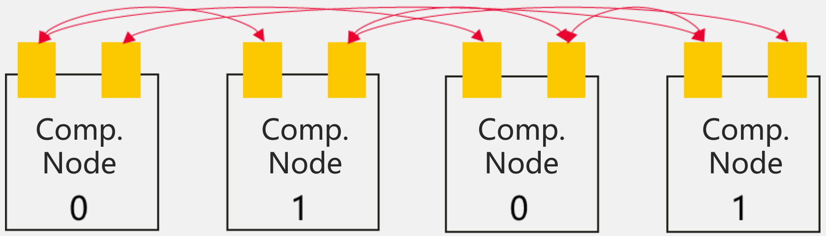
- **Features supported by the platform include:** UB-Next basic memory semantic protocol, short-path migration engine, composite semantic processing engine, low-latency switching, and other innovative functions.
  - **UB.mem**: Supports native memory semantic read/write operations, on-path/off-path acceleration logic, etc.
  - **UB-SSD**: FPGA-based SSD with memory semantic capabilities, near-data computing, etc.
  - **Low-latency Switching:** Packet-Cell Converged Switching Based on FPGA
- **Access:** Remote access provided via the Huang Danian platform and the laboratory.



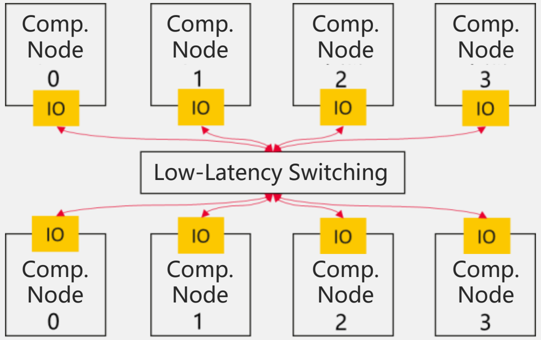
Multi-head Memory Pool Architecture



Direct Borrowing Topology Architecture



Switch-based Interconnect Architecture



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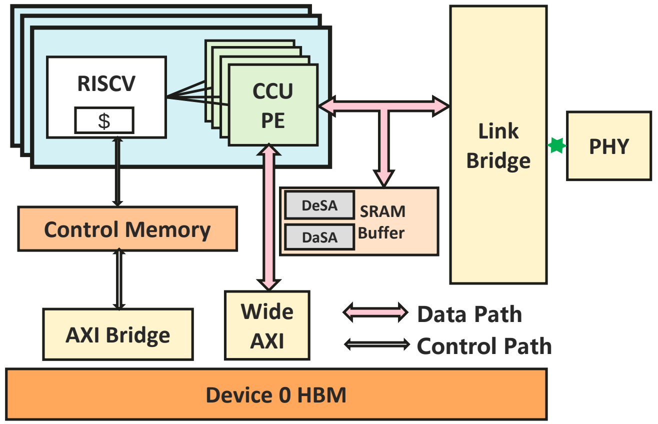
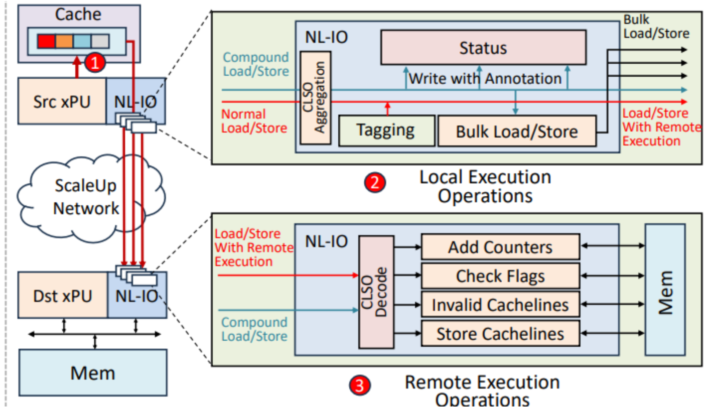
Exploration of Hardware-Software Co-Design Innovation Based on Scale-Up Prototype Platform

OpenCCU Collective Communication Accelerator



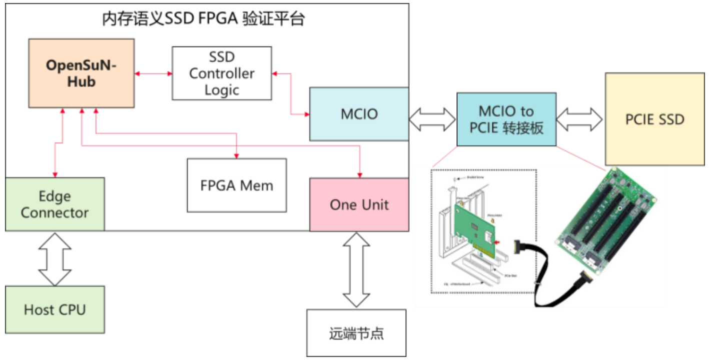
- **Multi-core RISC-V Architecture:** Based on RISC-V instruction set, parses collective communication instructions via parallel processing at the multi-core frontend.
- **Collective Communication Extension Instructions:** Extends collective instructions via the RoCC interface, supporting ops such as Reduce, LoadTensor, and StoreTensor.
- **Automatic Architecture Design Optimization:** Automatically optimizes parameters, identifying the optimal ratio of PEs to RV Cores.

Compound Memory Semantics Microarchitecture



- **Compound Memory Semantics Support:** Trigger multiple transactions (bulk transfer, sync, conditional ops) via a single Ld/St request.
- **On-path measurement:** Measures remote memory traffic and identifies hot pages/conflicts, enabling SW/HW co-optimization for hierarchical memory.

Memory Semantics UB SSD



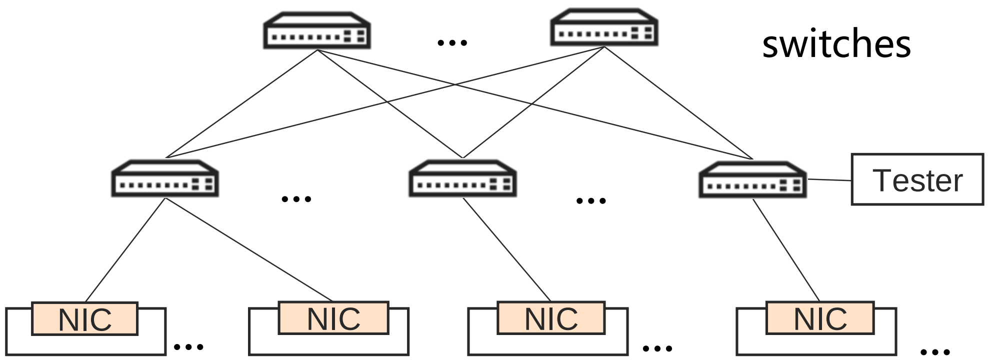
- **FPGA exposes host memory semantics:** Manages FPGA memory as SSD cache, supporting host semantic access.
- **Near-storage computing:** Handles compression/decompression, encryption/decryption, and matrix computation.
- **GPU passthrough:** Enables GPU/NPU passthrough to directly initiate SSD access.
- **NVMe-oF Target offloading:** SSDs act as target nodes for network access.

Scale-Out Prototype Platform: Supporting Innovation in Protocols and Algorithms for Scale-Out Networks

Fundamental Capabilities

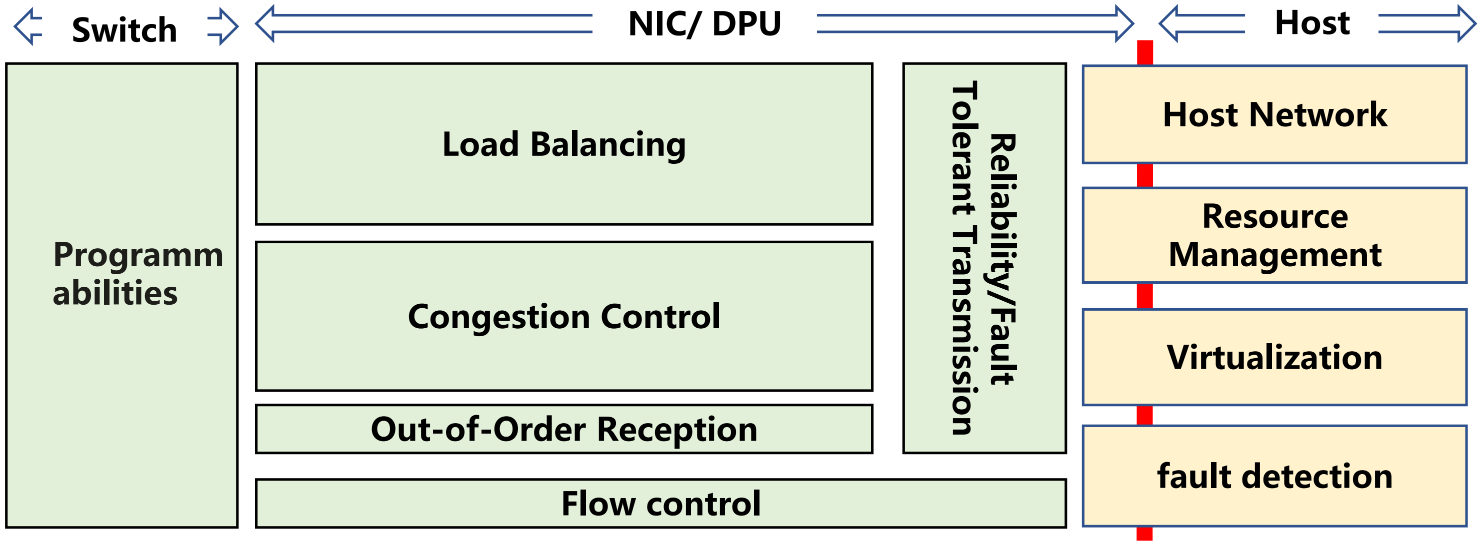
- **Basic components:** 10+ NICs, 10+ switches. 2-layer Clos architecture; supports other common topologies.
- **Programmability:** Programmable NICs and switches.
- **Protocol Capabilities:** UBoE and standard RoCE. Supports UB TP/TPG, multipath, packet spraying, out-of-order reception, congestion control, and lossless/lossy modes.
- **Access:** Remote access provided via the Huang Danian platform and the laboratory.

Platform overview



Platform-Enabled Innovation Capabilities

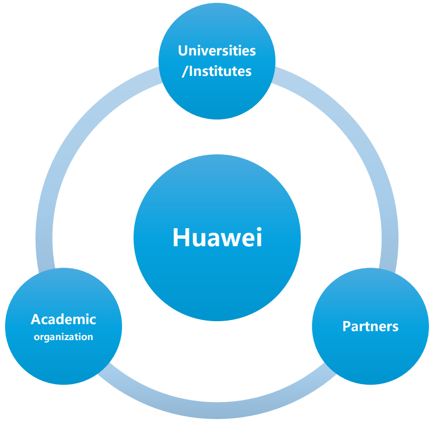
- **Focuses on protocol and algorithm innovation**
  - Per-packet load balancing
  - multi-path transmission
  - Congestion control
  - Packet trimming
  - Flow Control
  - Virtualization, etc.
- **New features coming soon, including NIC architecture, compute system**

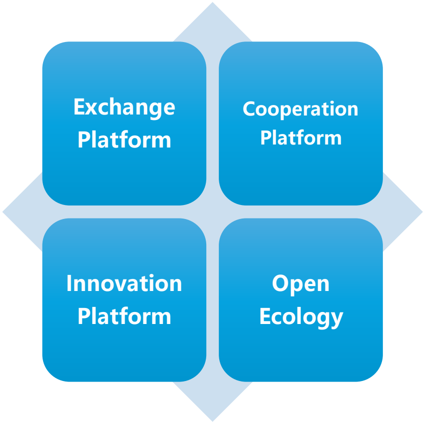


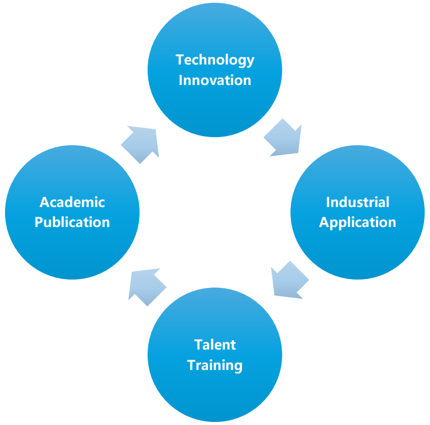
CompuNet: A Summit Focused on Computing Networks

- **CompuNet** aims to build an open platform for exchange and innovation, fostering technological breakthroughs and industrial progress in computing networks while contributing to academic development and talent cultivation.
- **The 2nd CompuNet Summit** was successfully held by Huawei and academic partners on Oct. 15, 2025.
  - The CompuNet Scale-Up Network Innovation Platform was officially released as **the industry's first open innovation platform** dedicated to Scale-Up networks.
  - A strategic collaboration was launched between **CompuNet** and the **CCF** (TCDCS, TCHPC, & TCI) to deepen industry-academia-research synergy. This initiative will explore cooperation through seminars, competitions, and academic courses, promoting cross-disciplinary innovation in Scale-Up networks across multiple computer science subfields.

Organization → **Platform** → **Achievements**







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Thank you.

把数字世界带入每个人、每个家庭、
每个组织，构建万物互联的智能世界。

Bring digital to every person, home and organization for a fully connected, intelligent world.

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